What is claim d is:

1. A nonvolatile semiconductor memory device comprising a plurality of memory elements formed in the vicinity of the surface of a substrate, a plurality of word lines for driving the memory elements, and a plurality of bit lines,

each of said plurality of memory elements including:

a semiconductor channel forming region formed in the vicinity of the surface of the substrate,

a source region in contact with the channel forming region in the vicinity of the surface of the substrate,

a drain region in contact with the channel forming region at a position facing the source region in the vicinity of the surface of the substrate,

a gate insulating film including a tunnel insulating film formed on the channel forming region,

a conductive gate electrode formed on the gate insulating film, and

a charge storing means which is provided in the tunnel insulating film and in the gate insulating film and is planarly dispersed to the other neighbor charge storing means in the gate insulating film;

a gate electrode of the plurality of memory

elements being respectively connect d to the plurality of word lines;

a gate insulating film formed on the semiconductor channel forming region and comprising a Fowler-Nordheim (FN) type tunneling film which has a FN type tunneling electroconductivity and contains material having a dielectric constant greater than that of silicon oxide;

a gate electrode formed on the gate insulating film; and

a charge storing means, formed in the gate insulating film, and facing to the surface of the channel forming region.

2. A nonvolatile semiconductor memory device according to claim 1, wherein the FN tunneling film comprises any one of a nitride film, an oxynitride film, and aluminum oxide film, a tantalum pentaoxide film and a BST ($BaSrTiO_3$) film, having an FN tunneling electroconductivity.

3. A nonvolatile semiconductor memory device according to claim 1, wherein the gate insulating film includes a buffer layer formed between the FN tunneling film and the channel forming r gion and suppressing an interface trap level.

4. A nonvolatile semiconductor memory device

according to claim 1, wh rein the gate insulating film comprises a Pool-Frenkel (PF) type film including any one of a nitride film, an oxynitride film, and aluminum oxide film, a tantalum pentaoxide film and a BST ($BaSrTiO_3$) film, having ~~an~~ a PN type electroconductivity.

5. A nonvolatile semiconductor memory device according to claim 4, wherein the gate insulating film includes a buffer layer formed between the FN tunneling film and the PN film.

6. A nonvolatile semiconductor memory device according to claim 1, further comprising:

a pull-up electrode in the vicinity of the gate electrode or a wiring layer connected to the gate electrode, via a dielectric film; and

a pull-up gate bias means for applying a voltage to the pull-up electrode.

7. A nonvolatile semiconductor memory device according to claim 6, wherein

a plurality of gate electrodes of the plurality of memory transistors are connected to a plurality of word lines, and

a selected transistor is connected between the pull-up gate bias means and the pull-up electrode, said pull-up gate bias means supplying a voltage having a polarity same as a polarity of a boosting voltage for

boosting the precharged word line by a capacitance coupling.

E1

8. A nonvolatile semiconductor memory device according to claim 6, wherein the pull-up electrode is arranged in the vicinity of an upper portion of the gate electrode or a connection layer connected to the gate electrode, via the dielectric film.

9. A nonvolatile semiconductor memory device according to claim 1, wherein each memory transistor comprises a source region contracted to the channel forming region, and a drain region spaced to the source region and contacted to the channel forming region,

wherein a plurality of gate electrodes of the plurality of memory transistors are connected to a plurality of word lines,

wherein the source region and drain region of each memory transistor are connected to a common line in a bit direction, electrically insulated to and intersecting ~~to~~ the word line, and

wherein said nonvolatile semiconductor memory device further comprises

a write inhibit voltage supply means for supplying a reverse-biased voltage to the source region and/or the drain region of the memory transistor the gate electrode of which is connected to the word line selected

at a writing, through the common line, to make the source region and/or the drain region in a reverse-biased state to the channel forming region, and

a non-selected word line biasing means for supplying a voltage to a non-selected word line at the writing, a polarity of the voltage being a polarity making the non-selected word line in a reverse biased state to the channel forming region.

10. A nonvolatile semiconductor memory device according to claim 9, wherein the write inhibit voltage supply means supplies the reverse bias voltage to the source region and/or the drain region to make a bias ~~a~~ voltage of the memory transistor connected to the selected word line to thereby prevent an erroneous write and/or an erroneous erase.

11. A nonvolatile semiconductor memory device according to claim 9, wherein the non-selected word line biasing means supplies a voltage having a polarity for reverse-biasing to the non-selected word line to make a bias ~~a~~ voltage of the memory transistor connected to the non-selected word line to thereby prevent an erroneous write and/or an erroneous erase.

12. A nonvolatile semiconductor memory devic according to claim 9, wh rein the non-selected word line biasing means a biases the gate electrode to the source

region so that a voltage of th gate electrode becomes a low level equal or lower than an inhibit gate voltage.

13. A nonvolatile semiconductor memory device according to claim 9, wherein when the reverse bias voltage is supplied to the channel forming region while the gate electrode and the channel forming region of the memory transistor are kept at a same potential level, depletion layers extend from the source region and drain region to the channel forming region to merge them.

14. A nonvolatile semiconductor memory device according to claim 9, wherein the gate length of the memory transistor is shorter than a gate length given by, when the reverse bias voltage is supplied while the gate electrode and the channel forming region are kept at a same potential level, ~~a~~ merged depletion layers extended from the source region and the drain region to the channel forming region.

15. A nonvolatile semiconductor memory device according to claim 1, wherein each memory transistor comprises a source region contacted to the channel forming region, and a drain region spaced to the source region and contacted to the channel forming region,

and wherein said nonvolatile semiconductor memory device comprises

a source line commonly connecting the plurality

of source regions of the plurality of memory transistors in a bit direction,

a bit line commonly connecting the plurality of drain regions of the plurality of memory transistors in the bit direction, and

a word line commonly connecting the plurality of gate electrodes of the plurality of memory transistors in a word direction.

16. A nonvolatile semiconductor memory device according to claim 1, wherein each memory transistor comprises a source region contacted to the channel forming region, and a drain region spaced to the source region and contacted to the channel forming region,

and wherein said nonvolatile semiconductor memory device comprises

sub source lines commonly connecting the plurality of source regions of the plurality of memory transistors in a bit direction,

a main source line commonly connecting the sub source lines in the bit direction,

sub bit lines commonly connecting the plurality of drain regions of the plurality of memory transistors in th bit direction,

a main bit line commonly connecting the sub bit line in the bit direction, and

a word lin commonly connecting the plurality of gate electrodes of the plurality of memory transistors in a word direction,

a selected memory transistor being connected between the sub source line and the main source line and between the sub bit line and the main bit line.

17. A nonvolatile semiconductor memory device according to claim 1, wherein the plurality of memory transistors are connected in series between a first selected transistor connected to a bit line and a second selected transistor connected to a common potential line.

18. A nonvolatile semiconductor memory device according to claim 1, wherein each memory transistor comprises a source region contacted to the channel forming region, and a drain region spaced to the source region and contacted to the channel forming region,

wherein said nonvolatile semiconductor memory device comprises

a plurality of element separation regions for isolating the respective memory transistors by insulation,

a common line commonly connecting the source regions or the drain regions in a bit direction, and

a word line connecting the plurality of gate electrodes in a word direction,

wherein the plurality of element separation regions are formed as lines along the bit direction and spaced from each other, and

wherein the common line intersects and is electrically isolated to the word line, is connected to one of the source region or the drain region, and is wired on the element separation regions by avoiding a wiring passing on another region of the source region or the drain region which is not connected to the common line.

19. A nonvolatile semiconductor memory device according to claim 18, wherein the plurality of element separation regions are formed as parallel strips having a width approximately equal to that of the word line, adjacent strips being spaced as adjacent word lines,

wherein a self-aligned contact hole is formed on the source region and the drain region by using a sidewall insulation layer formed on sidewalls of the word line, and

wherein the common line wired on the element separation regions is commonly connected to the one region through the self-aligned contact hole and is wired by a winding manner in the bit direction.

20. A nonvolatile semiconductor memory device according to claim 1, wherein the charge storing means

does not have conductivity as a whole facing to the channel forming region when charges are not moved to the outside of the memory transistor.

21. A nonvolatile semiconductor memory device according to claim 20, wherein the gate insulating film comprises

a tunneling insulating film formed on the channel forming region, and

a nitride film or an oxide nitride film, formed on the tunneling insulating film.

22. A nonvolatile semiconductor memory device according to claim 20, wherein the gate insulating film comprises

a tunneling insulating film formed on the channel forming region, and

conductors including small sized conductive material, formed on the tunneling insulating film as the charge storing means and isolated from each other.

23. A process of producing a nonvolatile semiconductor memory device, including the steps of:

forming a drain region, a source region and a channel forming region arranged between the drain region and the source region and contacted to them;

forming a gate insulating film including a charge storing means formed on and facing the surface of

the channel forming r gion; and

forming a gate electrode on the gate insulating film,

said gate insulating film formation step including a step of forming a Fowler-Nordheim (FN) type tunneling film comprising material having an FN tunneling electroconductivity and having a dielectric constant larger than that of silicon oxide, and

said FN tunneling film forming step including a step of heating the FN tunneling film at a high temperature under an atmosphere of reduction gas and/or oxidation gas.

24. A process of producing a nonvolatile semiconductor memory device according to claim 23, wherein the FN tunneling film comprises any one of a nitride film, an oxynitride film, and aluminum oxide film, a tantalum pentaoxide film and a BST ($BaSrTiO_3$) film, having an FN tunneling electroconductivity.

25. A process of producing a nonvolatile semiconductor memory device according to claim 23, further including a step of forming a buffer layer formed between the FN tunneling film and the channel forming region and suppressing an interface trap level, before forming the FN tunneling film.

26. A process of producing a nonvolatile

semiconductor memory device according to claim 23, further including a step of forming a Pool-Frenkel (PF) type film including any one of a nitride film, an oxynitride film, and aluminum oxide film, a tantalum pentaoxide film and a BST ($BaSrTiO_3$) film, having an PF electroconductivity, on the FN tunneling film.

27. A process of producing a nonvolatile semiconductor memory device according to claim 25, further including a step of forming a PN film on the FN tunneling film via the buffer layer, said PN film comprising any one of a nitride film, an oxynitride film, an aluminum oxide film, a tantalum pentaoxide film and a BST ($BaSrTiO_3$) film, having a PF electroconductivity.

28. A method of writing data into a nonvolatile semiconductor memory device, said nonvolatile semiconductor memory device comprising: a substrate;

a plurality of memory transistors formed in the substrate and arranged in a word direction and a bit direction; a pull-up electrode, each memory transistor including: a semiconductor channel forming region formed in the substrate; a gate insulating film formed on the semiconductor channel forming region and comprising a Fowler-Nordheim (FN) type tunneling film which has a FN type tunneling electroconductivity and contains material having a dielectric constant gr ater than that of silicon

oxid ; a gate electrode formed on the gate insulating film; and a charge storing means, formed in the gate insulating film, and facing to the surface of the channel forming region, said pull-up electrode in the vicinity of the gate electrode or a wiring layer connected to the gate electrode via a dielectric film,

said writing method including a step of applying a voltage to the pull-up electrode to raise a potential of the gate electrode.

29. A method of writing data into a nonvolatile semiconductor memory device according to Claim 28, including a step of applying a program voltage equal or lower than 10V, to a gate electrode of the selected memory transistor.

30. A method of writing data into a nonvolatile semiconductor memory device according to claim 28, wherein the pull-up electrode is capacitive-coupled to the gate electrode or the wiring layer connected to the gate electrode, via the dielectric film.

31. A process of producing a nonvolatile semiconductor memory device according to claim 28, wherein the FN tunneling film comprises any one of a nitride film, an oxynitride film, and aluminum oxide film, a tantalum pentaoxide film and a BST ($BaSrTiO_3$) film, having an FN tunneling electroconductivity.

32. A m thod of writing data into a nonvolatile

semiconductor memory device according to claim 28, wherein the gate insulating film includes a buffer layer formed between the FN tunneling film and the channel forming region and suppressing an interface trap level.

33. A method of writing ~~dat~~ data into a nonvolatile semiconductor memory device according to claim 28, wherein the gate insulating film comprises a Pool-Frenkel (PF) type film including ~~any~~ one of a nitride film, an oxynitride film, and aluminum oxide film, a tantalum pentaoxide film and a BST ($BaSrTiO_3$) film, having an PF electroconductivity.

34. A method of writing data into a nonvolatile semiconductor memory device according to claim 33, wherein the gate insulating film includes a buffer layer formed between the FN tunneling film and the PN film.

35. A method of writing data into a nonvolatile semiconductor memory device according to claim 28, including the steps of:

supplying a reverse-biased voltage to the source region and/or the drain region of the memory transistor the gate electrode of which is connected to the word line selected at a writing, through the common lin , to mak the source region and/or the drain region in a reverse-biased state to the channel forming region, and

supplying a voltage to a non-selected word line at the writing, a polarity of the voltage being a polarity making the non-selected word line in a reverse-biased state to the channel forming region.

36. A method of writing data into a nonvolatile semiconductor memory device according to claim 35, including a step of supplying the reverse-bias voltage to the source region and/or the drain region to make a bias ~~a~~ voltage of the memory transistor connected to the selected word line to thereby prevent an erroneous write and/or an erroneous erase.

37. A method of writing data into a nonvolatile semiconductor memory device according to claim 35, including a step of supplying a voltage having a polarity for reverse-biasing to the non-selected word line to make a bias ~~a~~ voltage of the memory transistor connected to the non-selected word line to thereby prevent an erroneous write and/or an erroneous erase.

38. A method of writing data into a nonvolatile semiconductor memory device according to claim 35, including a step of biasing the gate electrode to the source region so that a voltage of the gate electrode becomes a low level equal or lower than an inhibit gate voltage.

39. A method of writing data into a nonvolatile

semiconductor memory device according to claim 35, wherein when the reverse bias voltage is supplied to the channel forming region, the gate electrode and the channel forming region of the memory transistor are applied by a same voltage.

40. A method of writing data into a nonvolatile semiconductor memory device, wherein the reverse bias voltage is applied to the source region via a source line commonly connecting the source regions in the bit direction, and/or, the drain region via a bit line commonly connecting the drain regions in the bit direction, and

wherein the voltage having a polarity for reverse-biasing is applied via the word line commonly connecting the gate electrodes in the word direction.

41. A method of writing data into a nonvolatile semiconductor memory device according to claim 28, wherein each memory transistor comprises a source region contacted to the channel forming region, and a drain region spaced to the source region and contacted to the channel forming region,

and wherein said nonvolatile semiconductor memory device comprises

a source line commonly connecting th plurality of source regions of the plurality of m mory transistors

in a bit direction,

a bit line commonly connecting the plurality of drain regions of the plurality of memory transistors in the bit direction, and

a word line commonly connecting the plurality of gate electrodes of the plurality of memory transistors in a word direction.

42. A method of writing data into a nonvolatile semiconductor memory device according to claim 28, wherein each memory transistor comprises a source region contacted to the channel forming region, and a drain region spaced to the source region and contacted to the channel forming region,

and wherein said nonvolatile semiconductor memory device comprises

sub source lines commonly connecting the plurality of source regions of the plurality of memory transistors in a bit direction,

a main source line commonly connecting the sub source lines in the bit direction,

sub bit lines commonly connecting the plurality of drain regions of the plurality of memory transistors in th bit direction,

a main bit line commonly conn cting the sub bit line in the bit direction, and

a word line commonly conn cting the plurality of gate electrodes of the plurality of memory transistors in a word direction,

a selected memory transistors being connected between the sub source and the main source line and between the sub bit line and the main bit line.

43. A method of writing data into a nonvolatile semiconductor memory device according to claim 28, wherein the plurality of memory transistors are connected in series between a first selected transistor connected to a bit line and a second selected transistor connected to a common potential line.

44. A method of writing data into a nonvolatile semiconductor memory device according to claim 28, wherein each memory transistor comprises a source region contacted to the channel forming region, and a drain region spaced to the source region and contacted to the channel forming region,

wherein said nonvolatile semiconductor memory device comprises

a plurality of element separation regions for isolating the respective memory transistors by insulation,

a common line commonly connecting the source regions or the drain regions in a bit direction, and

a word line connecting the plurality of gate electrodes in a word direction,

wherein the plurality of element separation regions are formed as lines along the bit direction and spaced from each other, and

wherein the common line intersects and is electrically isolated to the word line, is connected to one of the source region or the drain region, and is wired on the element separation regions by avoiding a wiring passing on another region of the source region or the drain region which is not connected to the common line.

45. A method of writing data into a nonvolatile semiconductor memory device according to claim 44, wherein the plurality of element separation regions are formed as parallel strips having a width approximately equal to that of the word line, adjacent strips being spaced as adjacent word lines,

wherein a self-aligned contact hole is formed on the source region and the drain region by using a sidewall insulation layer formed on sidewalls of the word line, and

wherein the common line wired on the element separation regions is commonly connected to the one region through the self-aligned contact hole and is wired

by a manner in the bit direction.

46. A method of writing data into a nonvolatile semiconductor memory device according to claim 28, wherein the charge storing means does not have conductivity as a whole facing to the channel forming region when charges are not moved to the outside of the memory transistor.

47. A method of writing data into a nonvolatile semiconductor memory device according to claim 46, wherein the gate insulating film comprises

a tunneling insulating film formed on the channel forming region, and

a nitride film or an oxide nitride film, formed on the tunneling insulating film.

48. A method of writing data into a nonvolatile semiconductor memory device according to claim 46, wherein the gate insulating film comprises

a tunneling insulating film formed on the channel forming region, and

conductors including small sized conductive material, formed on the tunneling insulating film as the charge storing means and isolated from each other.

49. A m thod of writing data into a nonvolatile semiconductor m mory device according to claim 28, wherein a program voltage is applied to the gate

electrode, and

a voltage is applied to the pull-up electrode of the selected memory transistor.

50. A method of writing data into a nonvolatile semiconductor memory device according to claim 35, wherein a voltage having a polarity for reverse-biasing is applied to the non-selected word line,

the reverse-biasing voltage is applied to the source region and/or the drain region of the memory transistor connected to the selected word line,

a program voltage is applied to the selected word line, and

a voltage is applied to the pull-up electrode.

51. A method of writing data into a nonvolatile semiconductor memory device according to claim 50, wherein a selected memory transistor is connected to the word line and,

a selected memory transistor connected to a selected word line is controlled in a non-conductive state when the voltage is applied to the pull-up electrode.